REMARKS

Reconsideration and allowance are requested.

Claims 22-62 are now rejected under 35 U.S.C. §101 as allegedly being directed to non-statutory subject matter. This rejection is respectfully traversed.

Claims 22-42 have been amended to recite logic circuitry and to replace "operable" with "configured." Accordingly, the Examiner's concern that the claimed logic can be seen as an abstraction is no longer an issue. The term configured removes the concern with "intended use" the Examiner raises with respect to "operable." It is not understood how the term "comprising" can be viewed by the Examiner as an option, especially since it is probably one of the most common words used in patent claims.

Claim 43 as amended in the last response recites: "A computer program product including a storage medium readable by a data processing apparatus encoded with instruction code which, when executed by the data processing apparatus, controls the data processing apparatus to execute a sequence of variable length instructions stored within a plurality of discrete memory address regions within a memory of said data processing apparatus." The last response articulated why the claim is not to a program per se because the product includes instruction code embodied in a storage medium readable and executable by a data processing apparatus to achieve useful, concrete and tangible results. Applicants continue to believe claim 43 is statutory, that it does not recite a software program per se, and that it provides useful, concrete and tangible results. If the Examiner has a specific proposal to make this computer product claim more statutory, Applicants would be happy to consider it. Please provide your proposal via telephone to the undersigned at 703-816-4025.

Most of the claims remain rejected for anticipation under 35 U.S.C. §102 based on USP 5,598,544 to Ohshima. This rejection is respectfully traversed.

The technology of this application is directed to data processing systems that can execute a variable length instruction stored in distinct memory locations. The first part of a variable length instruction is stored in a first memory location, and the second part of the instruction is stored in a second different memory location. A "fix-up" memory address region is used to bring together the two parts of the single instruction. When a two-part, variable-length instruction occurs, the program execution flow is temporarily diverted to the fix-up memory to read the freshly reconstructed variable length instruction stored there. Thereafter, the program execution flow is returned to reading from the normal memory.

Ohshima is concerned with efficient processing of an instruction that includes both basic and expanded segments. A basic segment contains a code indicating the type of instruction (basic or expanded), and an expanded segment contains information relevant to the type of instruction specified by the basic segment. One instruction is formed from one or more basic and expanded segments. See column 3, lines 31-40. Even though the basic segments have a known length, the length of expanded segments can vary, and this length is not known until its corresponding basic segment has been decoded. Hence, in a situation where one of Ohshima's instructions consists of two basic segments and the first basic segment is followed by an expanded segment, the second basic segment cannot be input into a decoder until after the first basic segment has been decoded, which allows the length of the expanded segment to be determined. Thus, two cycles are required to decode the single instruction. See column 2, line 59 to column 3, line 9.

In the last response, Applicants explained why the claim element mapping onto Ohshima attempted by the Examiner was not reasonable. The Examiner maps the basis segments 1 and 2 shown in Figure 2 onto portions of a variable length instruction spanning two discrete memory address regions. The claimed concatenation is read onto Ohshima's wrapping of instructions within the instruction buffer 2 shown in Figure 4. As described above, Ohshima forms an expanded version of the instruction onto the instruction code bus ready for decoding and execution. The Examiner seems to be mapping this instruction code bus to the claimed fix-up memory address region. Applicants respectfully submit that a person skilled in the data processing art would not reasonably equate Ohshima's instruction code bus to the claimed fix-up memory address region—a bus and a memory are two different things with two different functions and operations.

The Examiner maps the claimed diverting and restoring to execution of an instruction on the instruction code bus and the execution of the next instruction. This mapping is also unreasonable. The instruction code bus is not part of the memory address space. Moreover, instruction decoding always takes place from Ohshima's instruction code bus, and as a result, there is no need to divert program execution flow to the instruction code bus or restore program execution flow from the instruction code bus.

The Examiner's comments in the last three lines of page 5 of the Office Action regarding the claimed fix-up memory address region and Ohshima's code bus are unclear. The rearrangement of instruction segments in Ohshima is performed by the "output selection circuit" 8 (see Figure 6A) in order to alter the order in which the segments appear on the instruction code bus (see Figure 6B). There is simply no reasonable interpretation of this arrangement in Ohshima which corresponds to "concatenating instruction data from an end portion of said

current memory address region and a start portion of said following memory address region into a fix-up memory address region of said memory," as recited by the independent claims.

On page 6, lines 1-4 of the Office Action, the Examiner appears to be arguing that the instruction code bus in Ohshima can be considered to be memory address space. But a person skilled in the art would not reasonably equate Ohshima's instruction code to the claimed fix up memory address region. The Examiner's arguments in lines 5-8 of page 6 of the Office Action are also unclear. Is the Examiner arguing that program execution flow is diverted and restored in Ohshima? If so, no reference to where this is described in Ohshima is provided. The remainder of page 6 of the Office Action is similarly unclear. Clarification and specific identification of the specific elements in Ohshima that allegedly correspond to the claim features are respectfully requested.

As a further distinction from Ohshima, the independent claims have been amended to further specify the feature of "said attempt triggering a memory abort." Example support for this amendment may be found at page 9, lines 16-23 of the specification. This claim feature is also not disclosed by Ohshima which makes no reference to memory aborts when attempting to execute a variable length instruction.

Accordingly, the application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

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